REMARKS

Applicants have studied the Office Action dated November 28, 2005 and have made amendments to the claims. It is submitted that the application, as amended, is in condition for allowance. By virtue of this amendment, claims 1, 5-8, 12-14, 18-19, and 23 are pending. Claims 2-4, 9-11, 15-17, and 20-22 have been cancelled without prejudice or disclaimer. Claims 1, 5, 8, 14, 19, and 23 have been amended. Reconsideration and allowance of the pending claims in view of the above amendments and the following remarks are respectfully requested.

Preferred embodiments of the present invention provide a circuit with a pipeline structure. The circuit has a sequence of functional units (stages) that work in parallel to perform a task in several steps. One embodiment of the circuit is shown below.

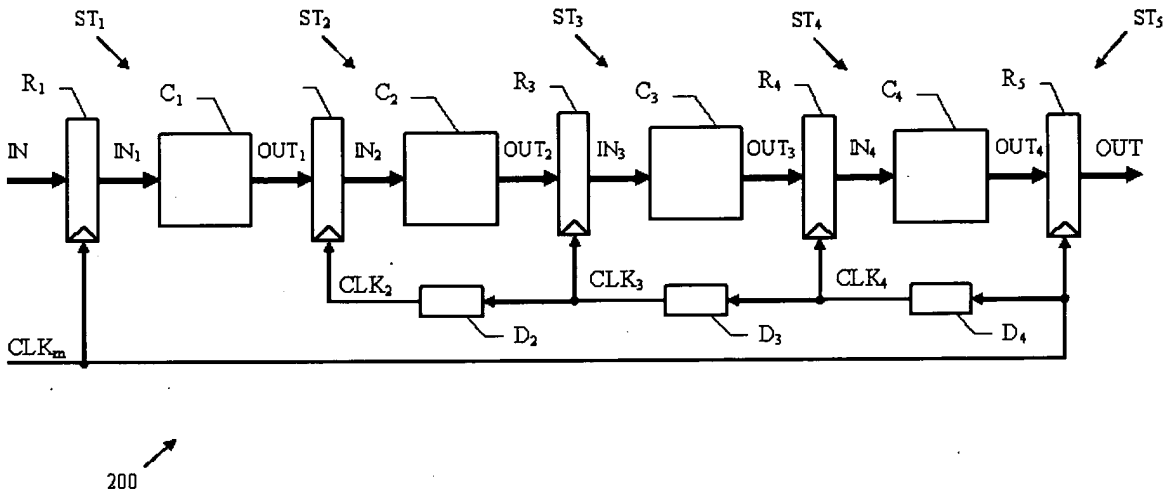


FIG.2

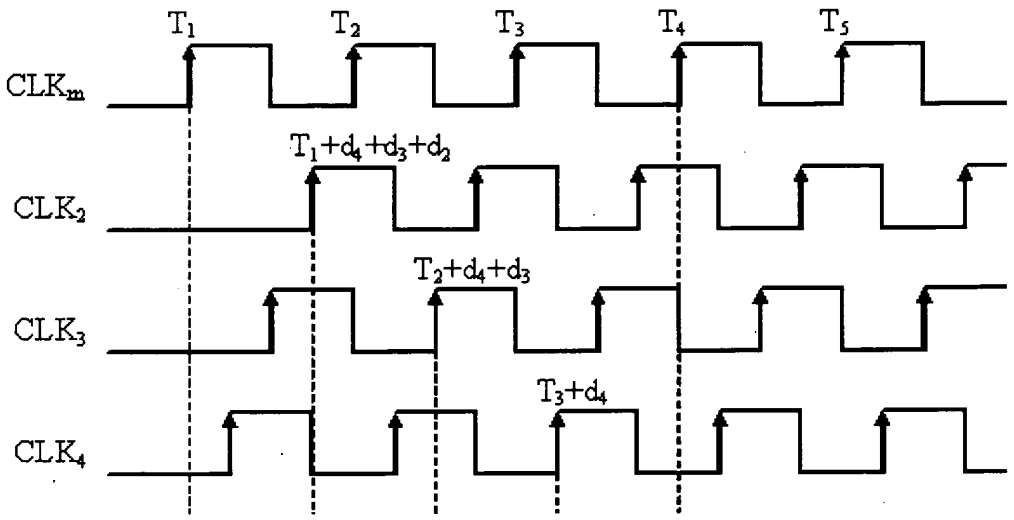
As shown, this circuit includes a set of stages ($ST_{1\text{-}5}$) that are arranged in a linear sequence. The first stage (ST_1) receives the input of the pipeline structure and the last stage (ST_5) provides an output of the pipeline structure. The first stage and the last stage are controlled by a main clock signal (CLK_m). The circuit also includes intermediate stages ($ST_{2\text{-}4}$) that are interposed between the first stage (ST_1) and the last stage (ST_5).

The circuit also includes a phase shifting circuit for generating a plurality of "local" clock signals, which each control a corresponding one of the intermediate stages. These local clock signals are produced by delay blocks (D_{2-4}) that each delay the clock signal that is fed to the adjacent stage in the sequence. Therefore, the local clock signals (CLK_{2-4}) are all generated from the main clock signal (CLK_m), but because they are each delayed by a delay (D_2, D_3, or D_4) from the adjacent stage, the main clock signal and the local clock signals are all out of phase with one another.

For example, in the embodiment described in paragraph 0026 of the present application, the local clock signal CLK_4 is obtained by applying the delay D_4 to the main clock signal CLK_m; the local clock signal CLK_3 is obtained by applying the delay D_3 to the local clock signal CLK_4 (i.e., the delay D_4+D_3 applied to the main clock signal CLK_m); and the local clock signal CLK_2 is obtained by applying the delay D_2 to the local clock signal CLK_3 (i.e., the delay $D_4+D_3+D_2$ applied to the main clock signal CLK_m).

Importantly, the delays produced in this circuit <u>begin</u> at the clock signal fed to the <u>last stage</u> ST_5 and then sequentially <u>move upstream</u> in the circuit, in contrast to the downstream movement of the input signal IN. As a result, as shown in the timing chart below, the first stage switches at a time T_1 (in response to the rising edge of the main clock signal CLK_m). The following stages then switch in succession at the next rising edge of the local clock signal CLK_2 (time $T_1+D_4+D_3+D_2$), at the next rising edge of the local clock signal CLK_3 (time $T_2-D_4+D_3$), at the next rising edge of the local clock signal CLK_4 (time T_3+D_4), and at the next rising edge of the main clock signal CLK_m (time T_4), respectively. See specification at Paragraph 0028.

As clearly shown in the figure below, this achieves relatively long time differences between each pair of adjacent clock signals through very short delays. Each delay block receives the clock signal of the next stage. **This makes it possible to ensure correct operation of the pipeline with shorter delays (than if the local clock signals were obtained from the previous stage).** See specification at page 9, lines 16-19. The corresponding delay blocks can then be implemented with a reduced number of logic gates, so as to greatly reducing the occupied area and power consumption. For example, in the exemplary pipeline circuit described in the specification, the time difference between the clock signals CLK_4 and CLK_m is almost equal to the period T of the main clock signal; however, this result is achieved by a very short delay D_4 (applied to the clock signal CLK_m). Likewise, a similar (long) time difference between the clock signals CLK_3 and CLK_4 is achieved through an additional short delay D_3, and so on.



Claims 1-7 and 19-23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Janssens et al. (U.S. Patent No. 6,122,751) in view of Neff (U.S. Patent No. 6,956,432 B2). This rejection is respectfully traversed.

Amended independent claim 1 recites:

> wherein for each of the intermediate stages, the phase shifting circuit includes a delay block for producing the local clock signal controlling that intermediate stage **from the clock signal controlling a next one of the stages in the sequence,**

the first stage and the last stage are controlled by a main clock signal,

the at least two local clock signals are generated from the main clock signal, and

the main clock signal and the at least two local clock signals are out of phase with one another. (emphasis added)

Amended independent claim 19 recites:

generating, with a delay block, at least two local clock signals from the main clock signal, the main clock signal and the at least two local clock signals being out of phase; and

controlling each of the at least two intermediate stages with a different one of the at least two local clock signals, wherein each of the local clock signals is out of phase with the other and is produced from a next one of the stages in the sequence. (emphasis added)

The Janssens reference discloses a pipeline circuit in which, in sharp contrast to the present invention, the different clock signals (18a-c) are generated **centrally** by a clock circuit (18) and then distributed to the stages 12a, 14, 16, and 12b directly from the clock circuit (18), as shown in FIG. 1. See Janssens at col. 2, line 66 to col. 3, line 5. As recognized by the Examiner, Janssens fails to disclose a pipeline wherein the first stage (STF) and the last stage (STL) are controlled by a main clock such that local intermediate clock signals to drive the intermediate stages (ST2 and ST3) are generated from said main clock signal. However, the Examiner went on to state that the Neff reference makes up for this deficiency in the disclosure of Janssens. This position of the Examiner is respectfully traversed.

As shown in FIG. 3A, Neff discloses a set of delays (42-1 through 42-4) connected in series. Each clock signal is obtained by incrementally delaying the clock signal generated by the previous delay stage in the chain. Neff at col. 3, lines 60-64. However, unlike the present invention, the object of Neff is to produce "a large number of interleaved clock signals with a small time delay Td between corresponding edges of adjacent ones of the interleaved clock signals." Neff at col. 1, lines 42-44.

The structure disclosed by Neff provides a completely different result as compared with embodiments of the present invention, because each stage in Neff delays the received clock signal only by a delay equal to the desired phase difference. Neff at col. 3, lines 43-45. Nowhere does Neff teach or suggest using the delay chain in an upstream configuration, as in the present invention.

By using the delay chain in an upstream configuration, the present invention makes it possible to ensure correct operation of the pipeline with shorter delays than if the local clock signals were obtained from the previous stage, as in the structure of Neff. See specification at page 9, lines 16-19. This allows the corresponding delay blocks to be implemented with a reduced number of logic gates, so as to greatly reduce the occupied area and power consumption.

More specifically, the specific object of Neff is to obtain small time delays between the clock signals (see Neff at col. 1, lines 40-45 and col. 4, lines 6-7). In contrast, by placing a delay chain in an upstream configuration, embodiments of the present invention allow relatively long time differences to be obtained between each pair of adjacent clock signals through the use of very short delays.

Nowhere does Neff teach or suggest using a delay chain in an upstream configuration. Therefore, Neff does not teach or suggest "a delay block for producing the local clock signal controlling that intermediate stage from the clock signal controlling a next one of the stages in the sequence," as recited in claims 1 and 19.

When there is no suggestion or teaching in the cited reference, the suggestion cannot come from the Applicant's own specification. The Federal Circuit has repeatedly warned against using the Applicant's disclosure as a blueprint to reconstruct the claimed invention out of isolated teachings of the prior art. See MPEP § 2143; *Grain Processing Corp. v. American Maize-Products*, 840 F.2d 902, 907, 5 USPQ2d 1788 1792 (Fed. Cir. 1988); *In re Fitch*, 972 F.2d 160, 12 USPQ2d 1780, 1783-84 (Fed. Cir. 1992). The Janssens reference, taken alone or in combination with Neff, does not suggest, teach, or even mention a delay block for producing the local clock signal controlling that intermediate stage from the clock signal controlling a next one of the stages in the sequence. Accordingly, claims 1 and 19 distinguish over the Janssens and Neff references.

For at least the foregoing reasons, amended claims 1 and 19 distinguish over Janssens and Neff. Further, claims 5-7 and 23 depend from claims 1 and 19, respectively, and thus claims 5-7 and 23 also distinguish over Janssens and Neff. Therefore, it is respectfully submitted that this rejection should be withdrawn.

Claim 8 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Allen (U.S. Patent No. 5,909,638) in view of Janssens et al.

Amended independent claim 8 recites:

> wherein for each of the intermediate stages, the phase shifting circuit includes **a delay block for producing the local clock signal controlling that intermediate stage from the clock signal controlling a next one of the stages in the sequence,**
>
> the at least two local clock signals are **generated from the main clock signal**. (emphasis added)

As recognized by the Examiner, Allen and Janssens fail to teach a pipeline wherein the first stage (STF) and the last stage (STL) are controlled by a main clock such that local intermediate clock signals to drive the intermediate stages (ST2 and ST3) are generated from said main clock signal.

Therefore, by the Examiner's own conclusion, independent claim 8 distinguishes over Allen, taken alone or in combination with Janssens. Accordingly, it is respectfully submitted that this rejection should also be withdrawn.

Claims 8-13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Allen in view of Janssens et al. and Neff. This rejection is respectfully traversed.

Amended independent claim 8 recites:

> wherein for each of the intermediate stages, the phase shifting circuit includes **a delay block for producing the local clock signal controlling that intermediate stage from the clock signal controlling a next one of the stages in the sequence,**
>
> the at least two local clock signals are **generated from the main clock signal.** (emphasis added)

As recognized by the Examiner (on page 8 of the Office Action), Allen fails to disclose a digital system containing at least one pipeline structure wherein the pipeline structure comprises a phase shifting circuit for generating a least one local clock signal for controlling the at least one intermediate stage. Therefore, Allen cannot disclose that "for each of the intermediate stages, the phase shifting circuit includes a delay block for producing the local clock signal controlling that intermediate stage from the clock signal controlling a next one of the stages in the sequence," as recited in amended claim 8.

Further, as also recognized by the Examiner, Allen and Janssens et al. fails to disclose a pipeline wherein the first stage (STF) and the last stage (STL) are controlled by a main clock **such that local intermediate clock signals to drive the intermediate stages (ST2 and ST3) are generated from said main clock signal.**

Therefore, neither Allen nor Janssens teach *a delay block for producing the local clock signal controlling that intermediate stage from the clock signal controlling a next one of the stages in the sequence*, as recited in amended claim 8.

As explained above, the structure disclosed in Neff provides a completely different result as compared with embodiments of the present invention, because each stage in Neff delays the received clock signal only by a delay equal to the desired phase difference. Neff at col. 3, lines 43-45. More specifically, the specific object of Neff is to obtain small time delays between the clock signals (see Neff at col. 1, lines 40-45 and col. 4, lines 6-7). In contrast, by placing a delay chain in an upstream configuration, embodiments of the present invention allow relatively long time differences to be achieved between each pair of adjacent clock signals through very short delays.

Nowhere does Neff teach or suggest using a delay chain in an upstream configuration. Therefore, Neff does not teach or suggest "a delay block for producing the local clock signal controlling that intermediate stage from the clock signal controlling a next one of the stages in the sequence," as recited in claims 1 and 19.

When there is no suggestion or teaching in the cited reference, the suggestion cannot come from the Applicant's own specification. The Federal Circuit has repeatedly warned against using the Applicant's disclosure as a blueprint to reconstruct the claimed invention out of isolated teachings of the prior art. See MPEP § 2143; *Grain Processing Corp. v. American Maize-Products*, 840 F.2d 902, 907, 5 USPQ2d 1788 1792 (Fed. Cir. 1988); *In re Fitch*, 972 F.2d 160, 12 USPQ2d 1780, 1783-84 (Fed. Cir. 1992). The Allen reference, taken alone or in combination with Janssens and Neff, does not suggest, teach or even mention "for each of the intermediate stages, the phase shifting circuit includes a delay block for producing the local clock signal controlling that intermediate stage from the clock signal controlling a next one of the stages in the sequence."

For at least the foregoing reasons, amended claim 8 distinguishes over Allen, Janssens and Neff. Further, claims 12 and 13 depend from claim 8, and thus claims 12 and 13 also distinguish over Allen, Janssens and Neff. Therefore, it is respectfully submitted that this rejection should also be withdrawn.

Claim 14 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Lin et al. in view of Allen. This rejection is respectfully traversed.

Amended independent claim 14 recites:

> a digital system including **at least one pipeline structure**, the pipeline structure including:...
>
> **a phase shifting circuit for generating at least two local clock signals each for controlling a corresponding one of the at least two intermediate stages**, the at least one local clock signal being generated from the main clock signal, and the main clock signal and the at least two local clock signals being out of phase,
>
> wherein for each of the intermediate stages, the phase shifting circuit includes a delay block for producing the local clock signal controlling that intermediate stage **from the clock signal controlling a next one of the stages in the sequence**. (emphasis added)

As recognized by the Examiner, Lin and Allen fail to teach an electronic device comprising a digital system containing at least one pipeline structure wherein the pipeline structure comprises a phase shifting circuit for generating at least one local clock signal for controlling the at least one intermediate stage.

Therefore, by the Examiner's own conclusion, amended claim 14 distinguishes over Lin, taken alone or combination with Allen. Accordingly, it is respectfully submitted that this rejection should also be withdrawn.

Claim 14 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Lin et al. in view of Allen and Janssens et al.

Amended independent claim 14 recites:

> a phase shifting circuit for generating at least two local clock signals each for controlling a corresponding one of the at least two intermediate stages, the at least one local clock signal being generated from the main clock signal, and the main clock signal and the at least two local clock signals being out of phase,

wherein for each of the intermediate stages, the phase shifting circuit includes a delay block for producing the local clock signal controlling that intermediate stage **from the clock signal controlling a next one of the stages in the sequence**. (emphasis added)

As recognized by the Examiner, Lin and Allen fail to teach an electronic device comprising a digital system containing at least one pipeline structure wherein the pipeline structure comprises **a phase shifting circuit for generating at least one local clock signal for controlling the at least one intermediate stage**. However, the Examiner states that Janssens makes up for this deficiency by teaching a phase shifting circuit for generating at least one local clock signal for controlling the at least one intermediate stage.

However, as recognized by the Examiner, Lin, Allen, and Janssens fail to teach a pipeline wherein the first stage (STF) and the last stage (STL) are controlled by a main clock such that **local intermediate clock signals to drive the intermediate stages (ST2 and ST3) are generated from said main clock signal**.

Therefore, based on the Examiner's own conclusions, none of Lin, Allen or Janssens, or a combination thereof, disclose "**a phase shifting circuit for generating at least two local clock signals each for controlling a corresponding one of the at least two intermediate stages, the at least two local clock signals being generated from the main clock signal**, and the main clock signal and the at least two local clock signals being out of phase, wherein for each of the intermediate stages, the phase shifting circuit includes a delay block for producing the local clock signal controlling that intermediate stage from the clock signal controlling a next one of the stages in the sequence."

Therefore, by the Examiner's own conclusion, independent claim 14 distinguishes over these references. Accordingly, it is respectfully submitted that this rejection should also be withdrawn.

Claims 14-18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Lin et al. in view of Allen, Janssens et al. and Neff.

Amended independent claim 14 recites:

> a phase shifting circuit for generating at least two local clock signals each for controlling a corresponding one of the at least two intermediate stages, **the at least two local clock signals being generated from the main clock signal,** and the main clock signal and the at least two local clock signals being out of phase,
>
> wherein for each of the intermediate stages, the phase shifting circuit includes a delay block for producing the local clock signal controlling that intermediate stage **from the clock signal controlling a next one of the stages in the sequence**. (emphasis added)

As recognized by the Examiner, Lin, Allen, and Janssens fail to teach a pipeline wherein the first stage (STF) and the last stage (STL) are controlled by a main clock such that **local intermediate clock signals to drive the intermediate stages (ST2 and ST3) are generated from said main clock signal.**" However, the Examiner states that Neff makes up for this deficiency.

As explained above, the structure disclosed in Neff provides a completely different result as compared with embodiments of the present invention, because each stage in Neff delays the received clock signal only by a delay equal to the desired phase difference. Neff at col. 3, lines 43-45. More specifically, the object of Neff is to obtain small time delays between the clock signals (see Neff at col. 1, lines 40-45 and col. 4, lines 6-7). In contrast, by placing a delay chain in an upstream configuration, embodiments of the present invention allows relatively long time differences to be achieved between each pair of adjacent clock signals through very short delays.

Nowhere does Neff teach or suggest using a delay chain in an upstream configuration. Therefore, Neff does not teach or suggest "a delay block for producing the local clock signal controlling that intermediate stage from the clock signal controlling a next one of the stages in the sequence," as recited in claim 14.

When there is no suggestion or teaching in the cited references, the suggestion cannot come from the Applicant's own specification. The Federal Circuit has repeatedly warned against using the Applicant's disclosure as a blueprint to reconstruct the claimed invention out of isolated teachings of the prior art. See MPEP § 2143; *Grain Processing Corp. v. American Maize-Products*, 840 F.2d 902, 907, 5 USPQ2d 1788 1792 (Fed. Cir. 1988); *In re Fitch*, 972 F.2d 160, 12 USPQ2d 1780, 1783-84 (Fed. Cir. 1992). The Lin, Allen, and Janssens references, taken alone or in combination with Neff, do not suggest, teach or even mention "for each of the intermediate stages, the phase shifting circuit includes a delay block for producing the local clock signal controlling that intermediate stage from the clock signal controlling a next one of the stages in the sequence."

For at least the foregoing reasons, amended claim 14 distinguishes over Lin, Allen, Janssens, and Neff. Claim 18 depends from claim 14, and thus claim 18 also distinguishes over Lin, Allen, Janssens, and Neff. Accordingly, it is respectfully submitted that this rejection should also be withdrawn.

In view of the foregoing, it is respectfully submitted that the application and the claims are in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is invited to call the undersigned attorney at (561) 989-9811 should the Examiner believe a telephone interview would advance the prosecution of the application.

Respectfully submitted,

Date: April 28, 2006

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